

DETAILED DESCRIPTION

[0020] In the following detailed description, reference is made to the accompanying drawings. The drawings show specific examples in which the invention may be practiced. It is to be understood that the features and principles described with respect to the various examples may be combined with each other, unless specifically noted otherwise. In the description as well as in the claims, designations of certain elements as “first element”, “second element”, “third element” etc. are not to be understood as enumerative. Instead, such designations serve solely to address different “elements”. That is, e.g., the existence of a “third element” does not require the existence of a “first element” and a “second element”. A semiconductor body as described herein may be made from (doped) semiconductor material and may be a semiconductor chip or be included in a semiconductor chip. A semiconductor body has electrically connecting pads and includes at least one semiconductor element with electrodes.

[0021] Referring to FIG. 1, an arrangement for joining two joining members is illustrated. The arrangement comprises a first part **41** such as, e.g., an anvil. A first joining member **10** and at least one second joining member **20** may be arranged on the first part **41**. The first part **41** may provide a flat support surface **400**, for example, on which the joining members **10**, **20** may be arranged. Usually, the first joining member **10** is arranged on the support surface **400** of the first part **41**, and between the at least one second joining member **20** and the first part **41**. An electrically conductive connection layer **30** may be arranged between the first joining member **10** and the second joining member **20**. The electrically conductive connection layer **30** generally may be a layer of a metal powder, e.g., a silver powder.

[0022] The arrangement further comprises a second part **42**. The second part **42** may be configured to exert pressure to the joining members **10**, **20**, as is indicated with the arrows in FIG. 1. In this way, the at least one second joining member **20** is pressed against the first joining member **10**. For example, the second part **42** may comprise one or more punches. The second part **42** may be made of metal, for example. Punches comprising a metal or any other comparably hard materials are often also called hard punches.

[0023] Usually, the first part **41** and the second part **42** are heated during the process of joining the joining members **10**, **20**. Such a process often is a so-called sintering process. It is, however, also possible that only one of the first part **41** and the second part **42** is heated during the joining process or that heat is applied in any other way. A heating element **43** is exemplarily illustrated for the first part **41** in FIG. 1. A heating element, however, is not specifically illustrated for the second part **42** in the Figure. For example, at least one of the first and the second part **41** and **42** may be heated to up to 100° C., up to 200° C., up to 300° C. or even more. In this way, the first joining member **10** and the second joining member **20** which are in direct or indirect contact with the first part **41** and the second part **42**, respectively, are heated by the first part **41** and/or the second part **42** and the heat is further transferred via the joining members **10**, **20** to the connection layer **30**. The connection layer **30** is compacted during this process and subsequently forms a solid substance-to-substance bond between the two joining members **10**, **20**. Such sintering processes are generally known and, therefore, will not be described in further detail.

[0024] The first joining member **10** may be a semiconductor substrate, for example. Semiconductor substrates often include a dielectric insulation layer, a first metallization layer attached to the dielectric insulation layer, and a second metallization layer attached to the dielectric insulation layer. The dielectric insulation layer is disposed between the first and second metallization layers.

[0025] Each of the first and second metallization layers may consist of or include one of the following materials: copper; a copper alloy; aluminum; an aluminum alloy; any other metal or alloy that remains solid during the operation of the power semiconductor module arrangement. The semiconductor substrate may be a ceramic substrate, that is, a substrate in which the dielectric insulation layer is a ceramic, e.g., a thin ceramic layer. The ceramic may consist of or include one of the following materials: aluminum oxide; aluminum nitride; zirconium oxide; silicon nitride; boron nitride; or any other dielectric ceramic. For example, the dielectric insulation layer may consist of or include one of the following materials: Al_2O_3 , AlN , or Si_3N_4 . For instance, the substrate may, e.g., be a Direct Copper Bonding (DCB) substrate, a Direct Aluminum Bonding (DAB) substrate, or an Active Metal Brazing (AMB) substrate. Further, the substrate may be an Insulated Metal Substrate (IMS). An Insulated Metal Substrate generally comprises a dielectric insulation layer comprising (filled) materials such as epoxy resin or polyimide, for example. The material of the dielectric insulation layer may be filled with ceramic particles, for example. Such particles may comprise, e.g., Si_2O , Al_2O_3 , AlN , or BrN and may have a diameter of between about 1 μm and about 50 μm . The first metallization layer of an IMS may be a comparably thin copper layer (e.g., thickness of between 35 μm and 140 μm), and the second metallization layer may be a comparably thick aluminum or copper layer (e.g., thickness of between 0.6 mm and 2.0 mm), for example. The dielectric insulation layer generally comprises a high insulation resistance while, at the same time, having a low thermal conduction coefficient. The substrate, however, may also be a conventional printed circuit board (PCB) having a non-ceramic dielectric insulation layer. For instance, a non-ceramic dielectric insulation layer may consist of or include a cured resin.

[0026] The at least one second joining member **20** may comprise one or more semiconductor bodies, for example. Usually one or more semiconductor bodies are arranged on a semiconductor substrate. Each of the semiconductor bodies arranged on a semiconductor substrate may include a semiconductor component such as a diode, an IGBT (Insulated-Gate Bipolar Transistor), a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), a JFET (Junction Field-Effect Transistor), a HEMT (High-Electron-Mobility Transistor), or any other suitable controllable semiconductor element. One or more semiconductor components may form a semiconductor arrangement on the semiconductor substrate. In FIG. 1, two second joining members **20** are exemplarily illustrated. Any other number of second joining members **20**, however, is also possible.

[0027] The first joining member **10** comprising a semiconductor substrate and the at least one second joining member **20** comprising at least one semiconductor component, however, is only an example. According to another example, the at least one second joining member **20** comprises at least one semiconductor substrate that is arranged on a first joining member **10** comprising a base plate or heat